FIG. 1

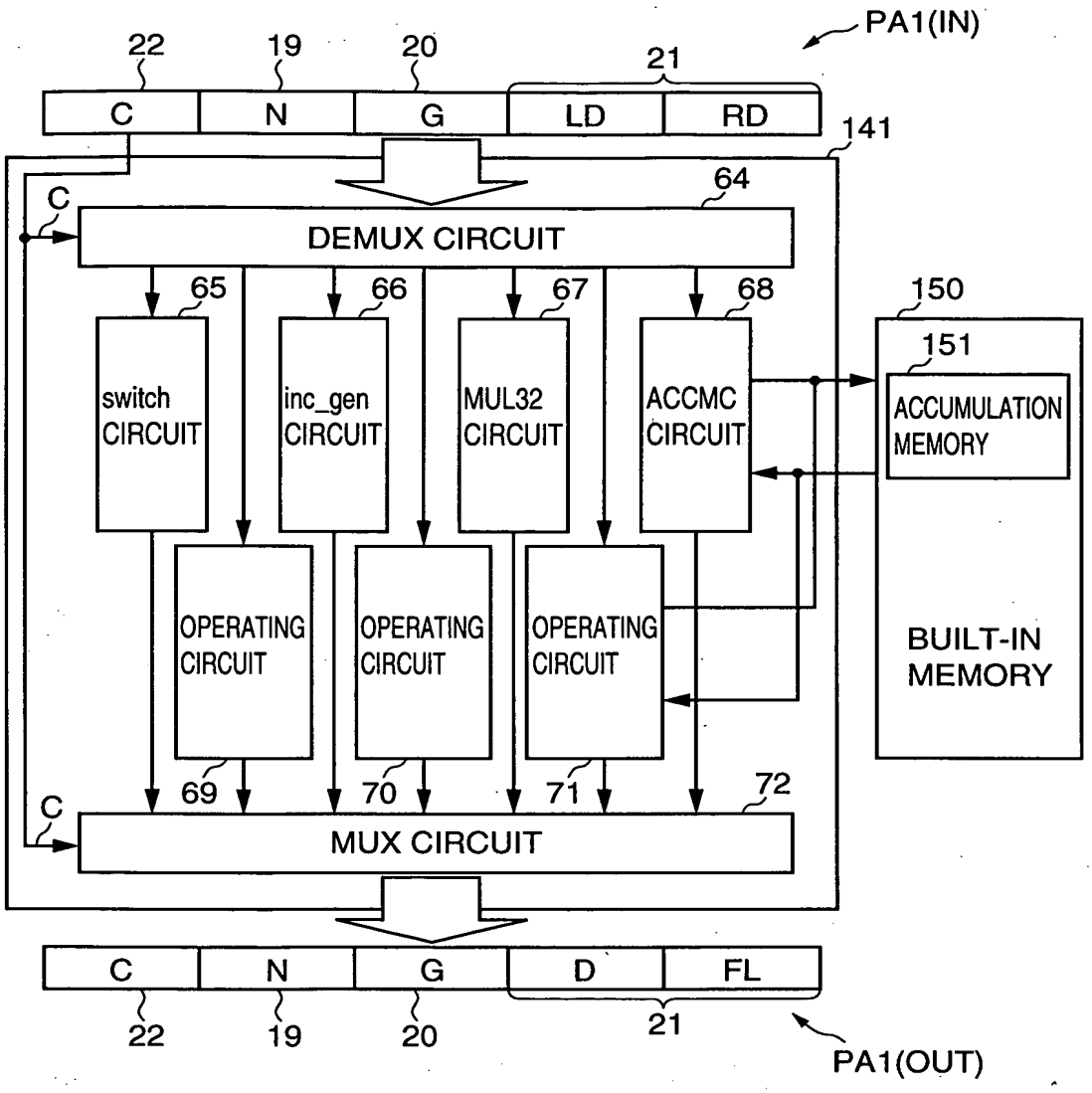
PA1(IN)
22
19
20
21
C
N
G
LD
RD
141
64
C
DEMUX CIRCUIT
65
66
67
68
150
151
switch CIRCUIT
inc_gen CIRCUIT
MUL32 CIRCUIT
ACCMC CIRCUIT
ACCUMULATION MEMORY
OPERATING CIRCUIT
OPERATING CIRCUIT
OPERATING CIRCUIT
BUILT-IN MEMORY
69
70
71
72
C
MUX CIRCUIT
C
N
G
D
FL
22
19
20
21
PA1(OUT)

FIG. 2

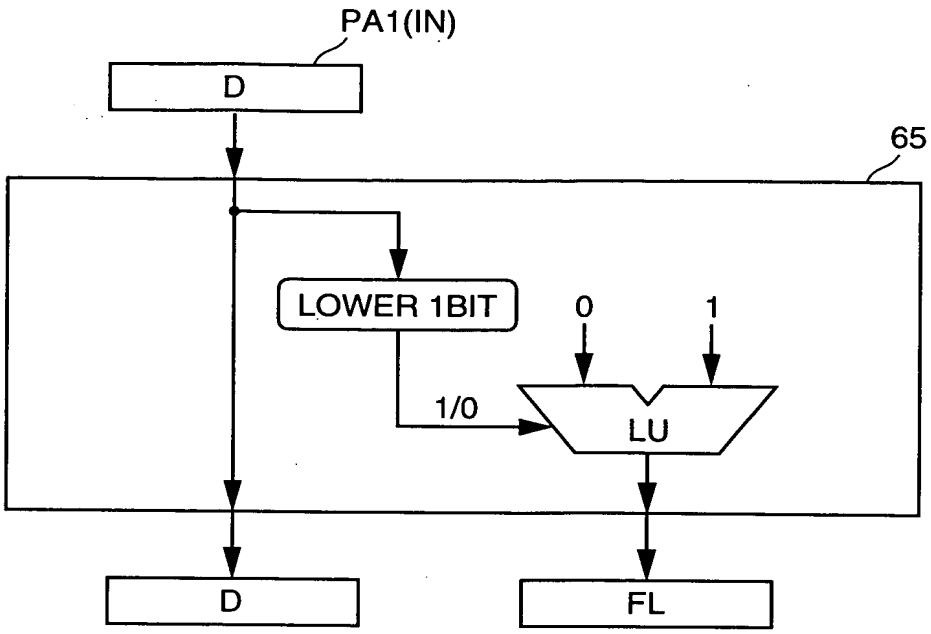
PA1(IN)
D
65
LOWER 1BIT
0
1
1/0
LU
D
FL

FIG. 3

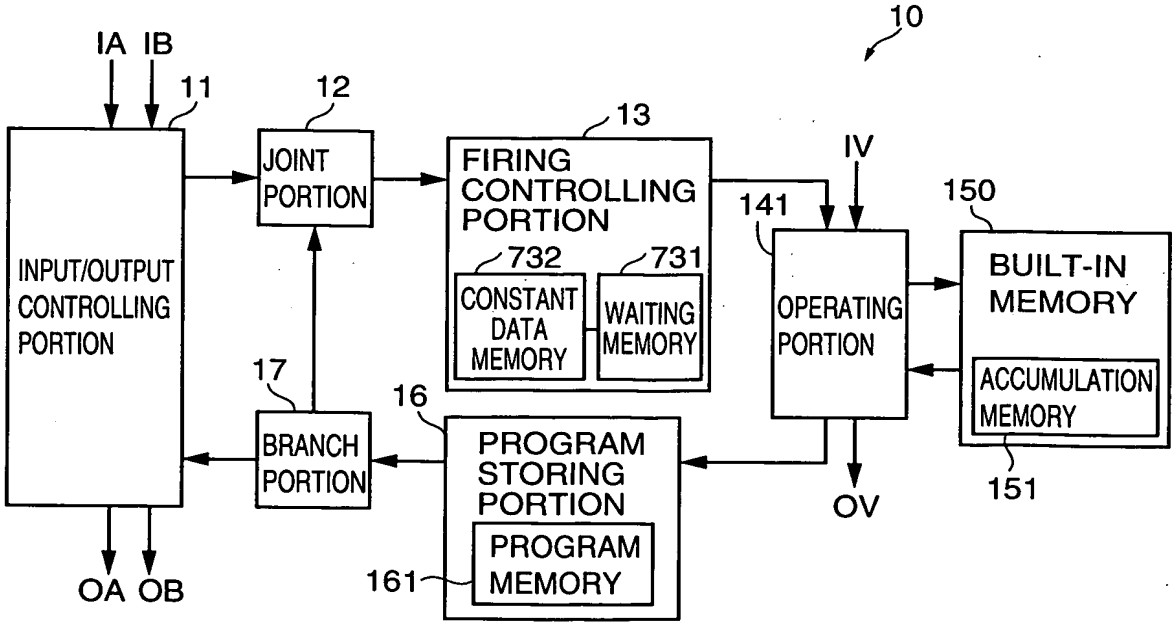
10
IA
IB
11
12
13
IV
141
150
INPUT/OUTPUT CONTROLLING PORTION
JOINT PORTION
FIRING CONTROLLING PORTION
732
731
CONSTANT DATA MEMORY
WAITING MEMORY
OPERATING PORTION
BUILT-IN MEMORY
ACCUMULATION MEMORY
17
16
BRANCH PORTION
PROGRAM STORING PORTION
PROGRAM MEMORY
161
OV
151
OA
OB

FIG. 4A

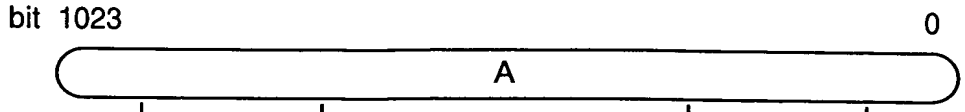

FIG. 4B

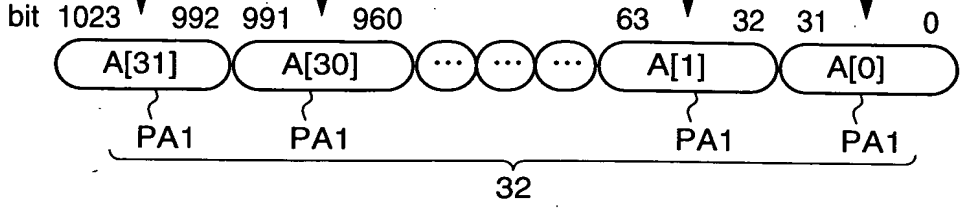

FIG. 5A

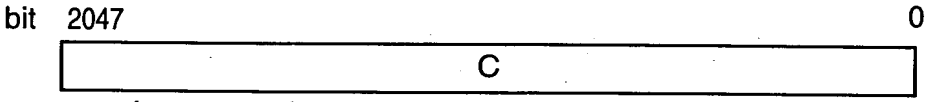

FIG. 5B

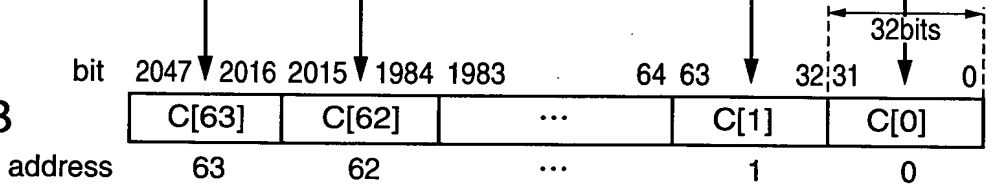

FIG. 6

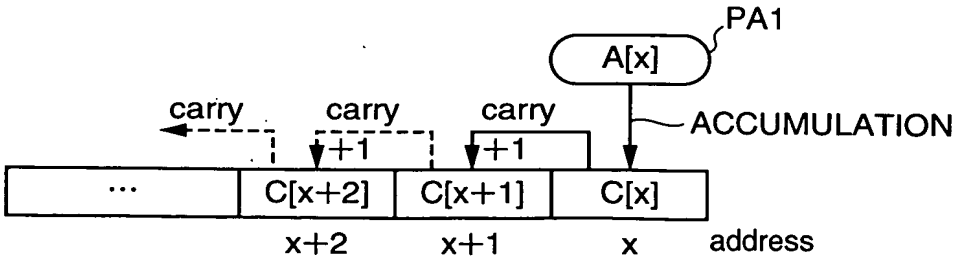

FIG. 7

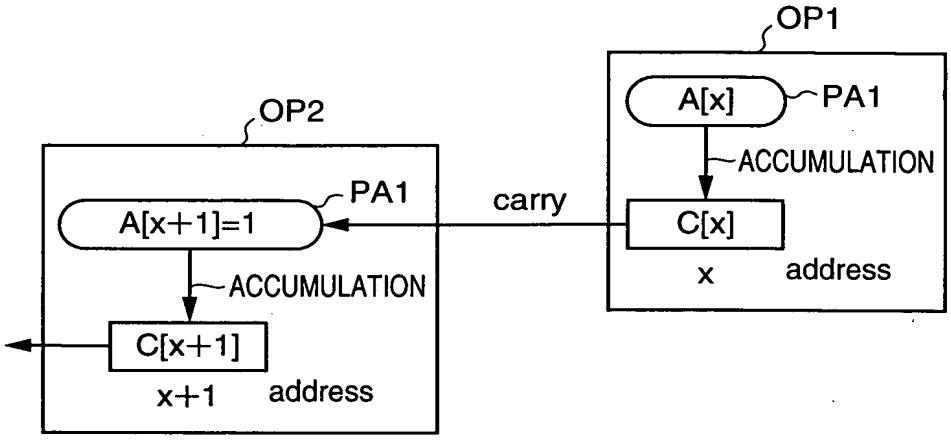

FIG. 8

$$
\begin{aligned}
C=A*B=&(A[0]*B[0]) + (A[0]*B[1])<<(32*1)\\
&+(A[0]*B[2])<<(32*2)+(A[0]*B[3])<<(32*3)\\
&+ \cdots\cdots + (A[0]*B[31])<<(32*31)\\
&+(A[1]*B[0])<<(32*1)+(A[1]*B[1])<<(32*2)\\
&+(A[1]*B[2])<<(32*3)+(A[1]*B[3])<<(32*4)\\
&+ \cdots\cdots + (A[1]*B[31])<<(32*32)\\
&+(A[2]*B[0])<<(32*2)+(A[2]*B[1])<<(32*3)\\
&+(A[2]*B[2])<<(32*4)+(A[2]*B[3])<<(32*5)\\
&+ \cdots\cdots + (A[2]*B[31])<<(32*33)\\
&\cdots\cdots\\
&\cdots\cdots\\
&+(A[31]*B[0])<<(32*31)+(A[31]*B[1])<<(32*32)\\
&+(A[31]*B[2])<<(32*33)+(A[31]*B[3])<<(32*34)\\
&+ \cdots\cdots + (A[31]*B[31])<<(32*62)
\end{aligned}
\qquad \text{EXPRESSION (1)}
$$

FIG. 9

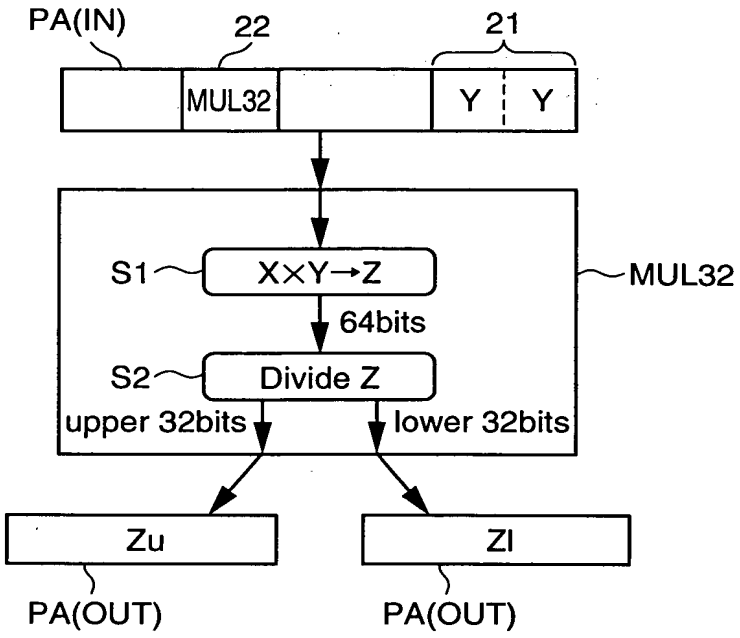
PA(IN)
22
21
MUL32
Y
Y
S1
X×Y→Z
MUL32
64bits
S2
Divide Z
upper 32bits
lower 32bits
Zu
Zl
PA(OUT)
PA(OUT)

FIG. 10

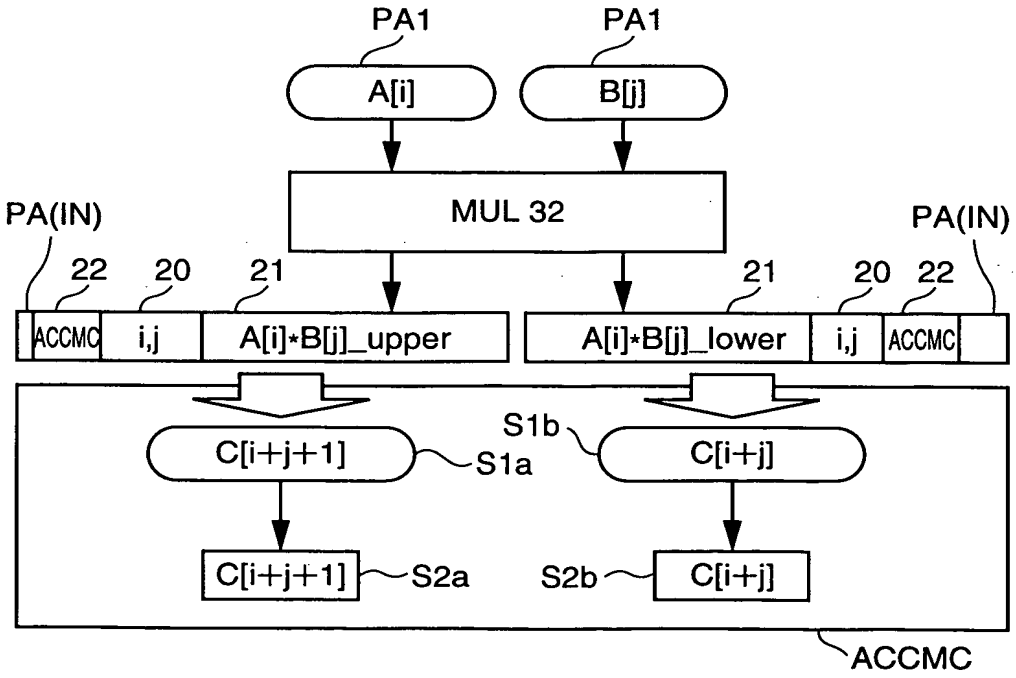
PA1
PA1
A[i]
B[j]
MUL 32
PA(IN)
PA(IN)
22
20
21
21
20
22
ACCMC
i,j
A[i]*B[j]_upper
A[i]*B[j]_lower
i,j
ACCMC
S1b
C[i+j+1]
S1a
C[i+j]
C[i+j+1]
S2a
S2b
C[i+j]
ACCMC

FIG. 11

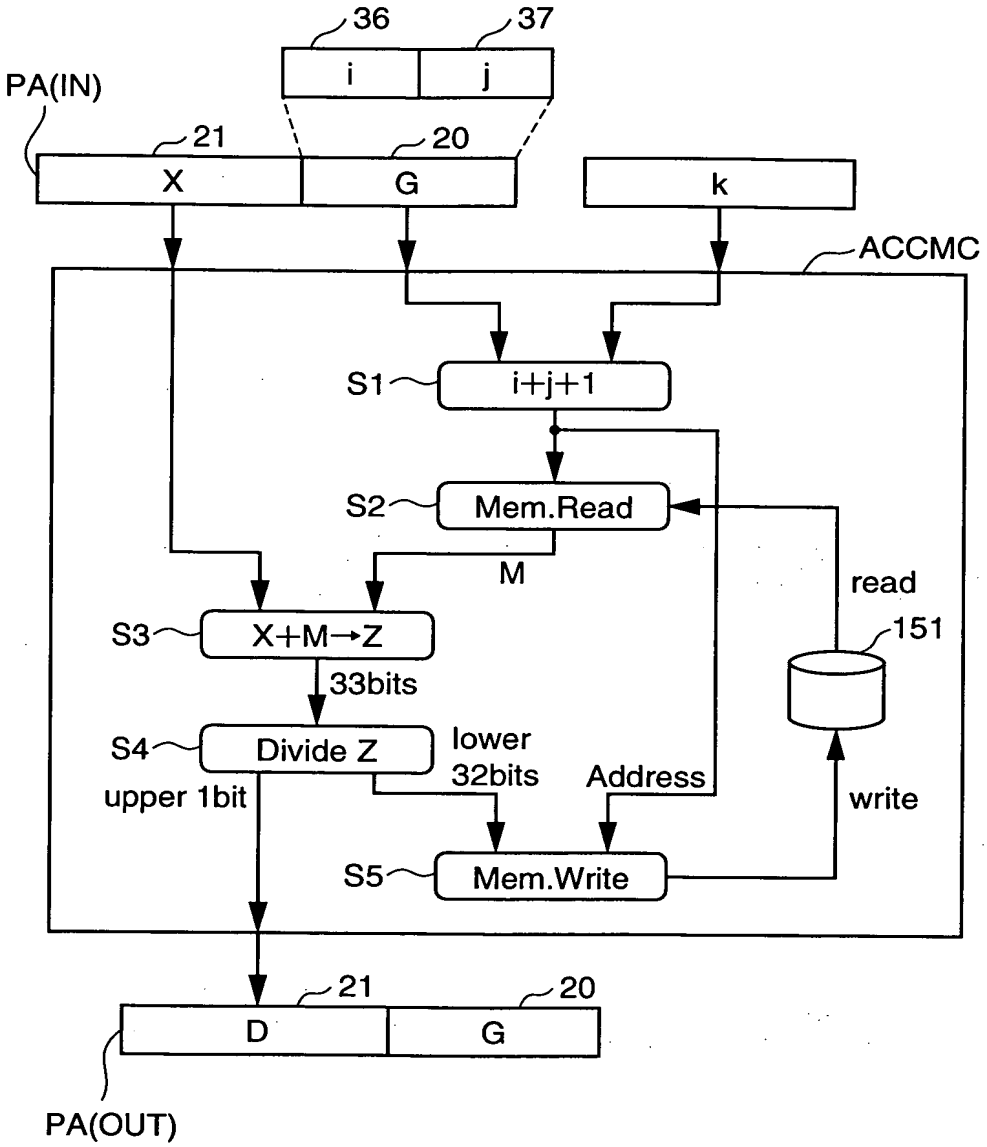
36
37
i
j
PA(IN)
21
20
X
G
k
ACCMC
S1
i+j+1
S2
Mem.Read
M
read
151
S3
X+M→Z
33bits
S4
Divide Z
lower
32bits
Address
upper 1bit
write
S5
Mem.Write
21
20
D
G
PA(OUT)

FIG. 12

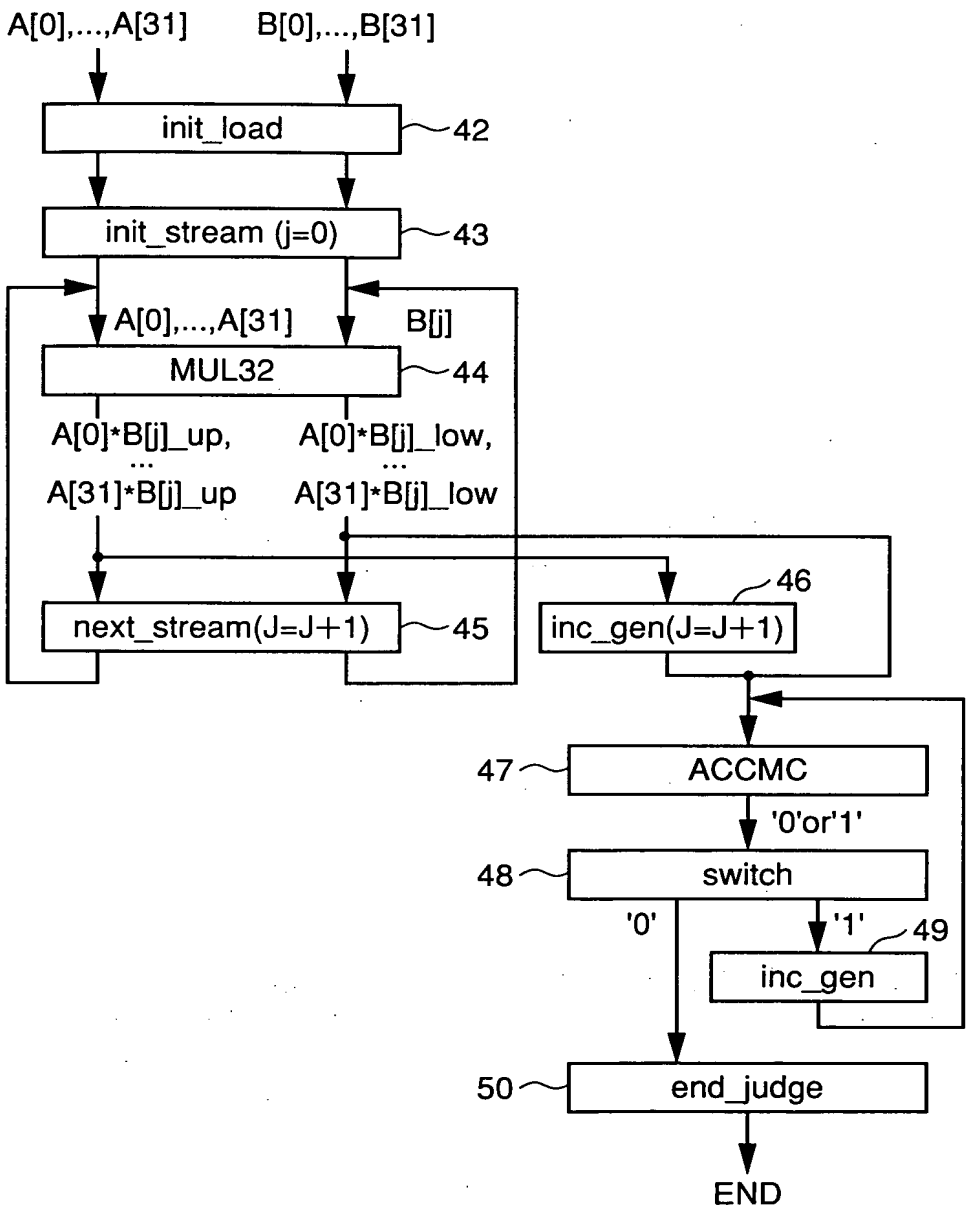
A[0],...,A[31]
B[0],...,B[31]
init_load
42
init_stream (j=0)
43
A[0],...,A[31]
B[j]
MUL32
44
A[0]*B[j]_up,
...
A[31]*B[j]_up
A[0]*B[j]_low,
...
A[31]*B[j]_low
next_stream(J=J+1)
45
46
inc_gen(J=J+1)
47
ACCMC
'0'or'1'
48
switch
'0'
'1'
49
inc_gen
50
end_judge
END

FIG. 13 PRIOR ART

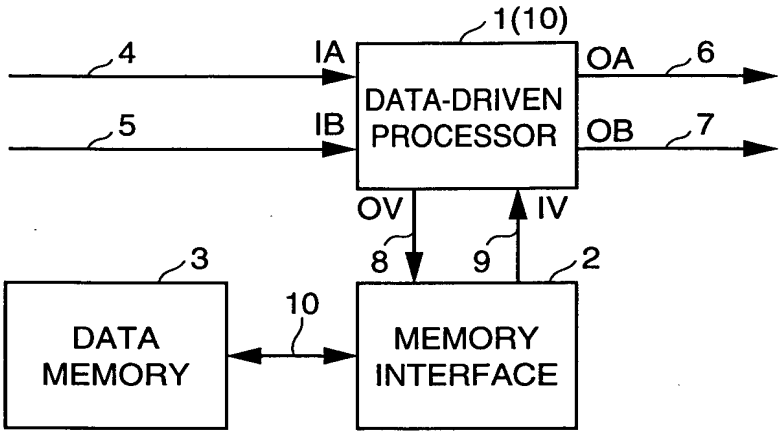

FIG. 14 PRIOR ART

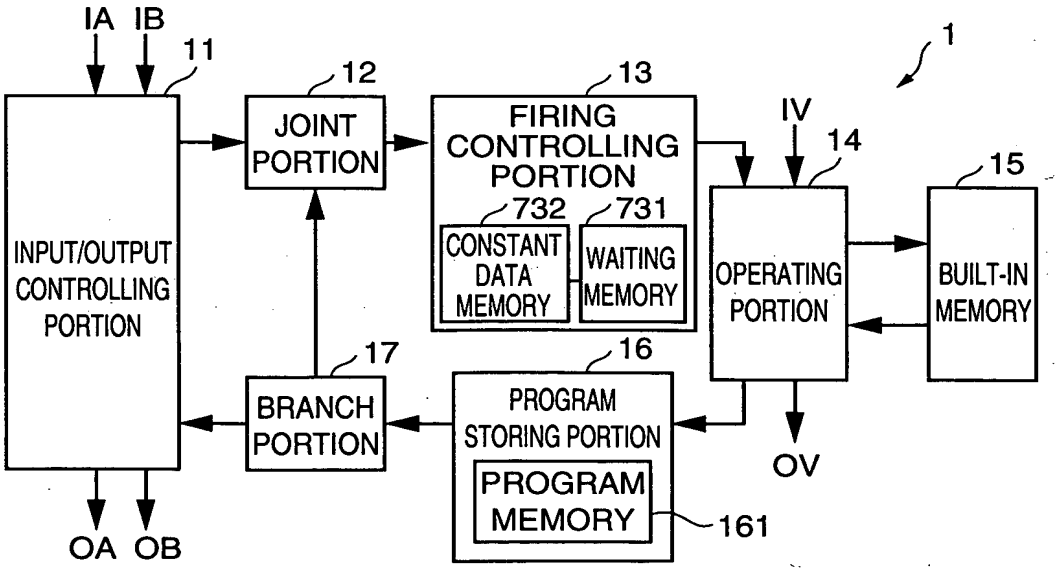

FIG. 15A PRIOR ART

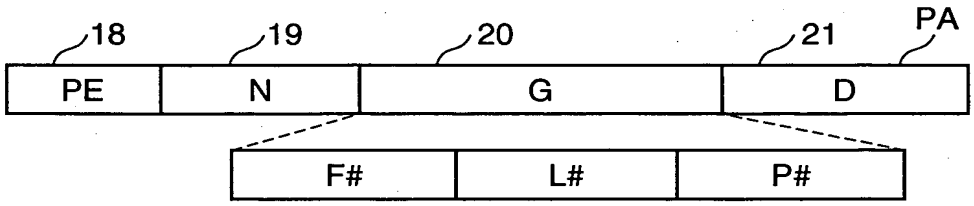

FIG. 15B PRIOR ART

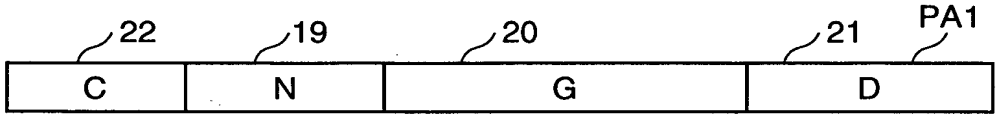

FIG. 16 PRIOR ART